AMENDMENT TO THE DRAWINGS:

The attached sheet of drawings includes new FIG. 7.

Attachment: New Sheet for FIG. 7.

REMARKS

STATUS OF THE DRAWINGS

The Office objected to the drawings under 37 CFR 1.83(a) as not showing at least one additional stacked layer on the thin chip. A new drawing sheet showing new FIG. 7 is included herewith. Support for this new figure is found throughout the Specification and, in particular, at page 8, line 24, through page 9, line 32; page 18, lines 14-15; and in Claim 2. *See* MPEP 608.01(l).

STATUS OF THE CLAIMS

Claims 1-12 remain in the application. Claims 13-16 have been withdrawn. Claims 2, 8 to 10, and 12 have been amended.

The Office rejected Claims 2, 8 to 10, and 12 under 35 USC 112, second paragraph, as being indefinite.

The Office rejected Claims 1, 3, 4, 6, 7, 9, 11, and 12 under 35 U.S.C. 102(e) as being anticipated by *Otsuka*.

The Office rejected Claims 1, 3, 4, and 6 to 12 under 35 U.S.C. 102(e) as being anticipated by *Ho*.

The Office rejected Claims 1, 3 to 7, 9, 11 and 12 under 35 U.S.C. 103(a) as being unpatentable over *Okabe*.

SUMMARY OF THE INVENTION

The present invention is directed to a microsystem-on-a-chip comprising a bottom wafer of normal thickness and a series of thinned wafers stacked on the bottom wafer, glued and electrically interconnected. The interconnection layer comprises a dielectric material, an interconnect structure, and can include embedded thin-film passives. The use of stacked, thinned silicon chips enables fully 3D, vertical integration. The stacked wafer technology provides a heterogeneously integrated, ultra-miniaturized, higher performing, robust and cost-effective microsystem package.

SUMMARY OF THE ART

Otsuka et al., U.S. 6,961,230, discloses a capacitor having a front surface on which a semiconductor device is mounted and a rear surface that is mounted on a surface of a circuit substrate. The capacitor provides power to the semiconductor device. A plurality of internal electrodes are disposed within the capacitor main body with a plurality of via conductors penetrating the main body to connect the front and rear surfaces and the internal electrodes. The circuit substrate core section comprises a glass-resin composite material having a plurality of through-hole conductors.

Ho et al., U.S. 6,865,089, discloses an integrated module board having embedded chips and components in cavities in a substrate mounted onto the module board. The substrate is bonded to a heat-dissipation sheet by an adhesion layer.

Okabe et al., U.S. 6,889,431, discloses an electronic circuit device comprising a multi-layer circuit incorporated within a thin film capacitor that can attain a higher capacitance value.

ARGUMENTS

CLAIMS 2, 8 TO 10, AND 12

The Office rejected Claims 2, 8 to 10, and 12 under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Specifically, the Office rejected Claim 2 asserting that it is unclear and confusing to what is meant by "further comprising at least one additional stacked layer on the thin chip..." Stacking of multiple thinned wafers is described throughout the specification and, in particular, at page 8, line 24, through page 9, line 32; page 18, lines 14-19; and in Claim 2 itself. Applicant has amended the drawing and description to show this subject matter. *See* MPEP 608.01(l).

Specifically, the Office rejected Claims 8-10 asserting that the phrase "the embedding passive" lacks proper antecedent basis. Applicant has amended Claims 8-10 to recite "the at least one passive component", which phrase has antecedent basis in Claim 7.

Specifically, the Office rejected Claim 12 asserting that the phrase "the on or more via" should probably be --the one or more via--. Applicant has amended Claim 12 to recite this proper phrase.

Applicant has amended the claims and submits that Claims 2, 8-10, and 12 are now in condition for allowance.

CLAIMS 1, 3, 4, 6, 7, 9, 11, AND 12, LIMITED TO A THIN UPPER CHIP COMPRISING ONE OR MORE MICROSYSTEM DEVICES CONNECTED BY VIAS IN AN INTERCONNECT LAYER TO ONE OR MORE MICROSYSTEM DEVICES ON A BOTTOM CHIP, ARE NOT ANTICIPATED BY *OTSUKA* UNDER 35 U.S.C. § 102(e)

The Office rejected Claims 1, 3, 4, 6, 7, 9, 11, and 12, asserting that the Applicant's microsystem-on-a-chip is anticipated by *Otsuka's* capacitor. To anticipate a claim, the reference must teach each and every element of the claim. *See* MPEP 2131. Applicant submits that *Otsuka* does not teach vertical integration of multiple chip layers.

Otsuka's element labeled **22** is a circuit substrate comprising a thick (800 μm) core section **23** of a glass-resin composite material having a plurality of through-hole conductors **27** between the front surface **24** and the rear surface **25**. *See Otsuka*, col. 10, line 35, through col. 11, line 3, and FIG. 4. The circuit **22** is not a bottom chip, as asserted by the Office. The circuit substrate **22** merely consists of through-hole conductors **27** that route power and signals from an external source to a semiconductor device **12** by way of an intermediate capacitor **1b**. *See Otsuka* col. 6, lines 45-53, and FIG. 5. In particular, the circuit substrate **22** does not comprise any microsystem devices, as asserted by the Office. Further, the element labeled **u1** is a first dielectric layer on a front side of capacitor **1b** consisting of via conductors **4** for transmitting and receiving signals between the semiconductor device **12** and the circuit substrate **22**. *See Otsuka*, col. 4, line 65, through col. 5, line 5; col. 5, lines 51-62; and col. 6, lines 45-65. In particular, the first dielectric layer **u1** is not a thin upper chip comprising one or more microsystem devices, as asserted by the Office.

Conversely, Applicant discloses and Claim 1 recites a three-dimensional, vertically integrated chip-stacking structure wherein microsystem devices (i.e., active components)

222 fabricated in the bottom chip **220** are connected to microsystem devices **242** fabricated in a thin upper chip **240** by an interconnect structure **238** in a compliant interconnect layer **230**. *See* Application pages 9-10, and FIG. 3.

With regards to claims 3 and 6, Applicant teaches that a thin interconnect layer (e.g., less than 50 microns) and a thin upper chip (e.g., less than 120 microns) are preferred to prevent thermal expansion mismatch between the stacked layers. *See* Application, page 9, lines 1-7, and page 10, lines 18-21.

Nowhere does *Otsuka* teach a bottom chip, comprising one or more microsystem devices, and a thin upper chip, comprising one or more microsystem devices, connected to the bottom chip through an interconnect layer, as recited in Applicant's Claim 1. Accordingly, Applicants submit that this rejection is overcome and that Claim 1 is in condition for allowance. Furthermore, Applicant submits that Claims 3, 4, 6, 7, 9, 11, and 12, that depend from and further define Claim 1, are likewise in condition for allowance. *See* MPEP 2143.03.

CLAIMS 1, 3, 4, AND 6 TO 12, LIMITED TO A THIN UPPER CHIP COMPRISING ONE OR MORE MICROSYSTEM DEVICES CONNECTED BY VIAS IN AN INTERCONNECT LAYER TO ONE OR MORE MICROSYSTEM DEVICES ON A BOTTOM CHIP, ARE NOT ANTICIPATED BY *HO* UNDER 35 U.S.C. § 102(e)

The Office rejected Claims 1, 3, 4, and 6 to 12, asserting that the Applicant's microsystem-on-a-chip is anticipated by *Ho's* module board. To anticipate a claim, the reference must teach each and every element of the claim. *See* MPEP 2131. Applicant submits that *Ho* does not teach vertical integration of multiple chip layers.

Ho's element labeled **31** is a heat-dissipation sheet, preferably a metal sheet like copper. *See Ho*, col. 3, lines 1-8; and FIGS. 1 and 12. The heat-dissipation sheet **31** is not a bottom chip, as asserted by the Office. In particular, the heat-dissipation sheet **31** does not comprise any microsystem devices, as asserted by the Office. Further, the elements labeled **42**, **46** are a dielectric layer and a mask layer comprising a metal wiring layer **44A** and solder balls **48**, respectively. *See Ho*, col. 4, lines 1-29, and FIG. 12. In

particular, the dielectric and mask layers **42**, **46** are not a thin upper chip comprising one or more microsystem devices, as asserted by the Office.

Conversely, Applicant discloses and Claim 1 recites a three-dimensional, vertically integrated chip-stacking structure wherein microsystem devices (i.e., active components) **222** fabricated in the bottom chip **220** are connected to microsystem devices **242** fabricated in a thin upper chip **240** by an interconnect structure **238** in a compliant interconnect layer **230**. *See* Application pages 9-10, and FIG. 3.

With regards to claims 3 and 6, Applicants teach that a thin interconnect layer (e.g., less than 50 microns) and a thin upper chip (e.g., less than 120 microns) are preferred to prevent thermal expansion mismatch between the stacked layers. *See* Application, page 9, lines 1-7, and page 10, lines 18-21.

Nowhere does *Ho* teach a bottom chip, comprising one or more microsystem devices, and a thin upper chip, comprising one or more microsystem devices, connected to the bottom chip through an interconnect layer, as recited in Applicant's Claim 1. Accordingly, Applicants submit that this rejection is overcome and that Claim 1 is in condition for allowance. Furthermore, Applicant submits that Claims 3, 4, and 6 to 12, that depend from and further define Claim 1, are likewise in condition for allowance. *See* MPEP 2143.03.

CLAIMS 1, 3 to 7, 9, 11, AND 12, LIMITED TO A THIN UPPER CHIP COMPRISING ONE OR MORE MICROSYSTEM DEVICES CONNECTED BY VIAS IN AN INTERCONNECT LAYER TO ONE OR MORE MICROSYSTEM DEVICES ON A BOTTOM CHIP, ARE NOT UNPATENTABLE OVER *OKABE* UNDER 35 U.S.C. § 103(a)

The Office rejected Claims 1, 3 to 7, 9, 11, and 12, asserting that the Applicant's microsystem-on-a-chip is anticipated by *Okabe's* module board. To establish a *prima facie* case of obviousness, *inter alia*, the prior art references must teach or suggest all of the claim limitations. *See* MPEP 2143. Applicant submits that *Okabe* does not teach or suggest vertical integration of multiple chip layers.

Okabe's element labeled **23** is a dielectric layer comprising an epoxy resin. *See Okabe*, col. 9, lines 22-42; and FIG 2. The dielectric layer **23** is not a bottom chip, as asserted by the Office. In particular, the dielectric layer **23** does not comprise any microsystem devices, as asserted by the Office. Further, the element labeled **21, upper portion of 22** is a base substrate. *See Okabe*, col. 6, lines 1-10, and FIG. 1. In particular, the base substrate **21, upper portion of 22** is not a thin upper chip comprising one or more microsystem devices, as asserted by the Office.

Conversely, Applicant discloses and Claim 1 recites a three-dimensional, vertically integrated chip-stacking structure wherein microsystem devices (i.e., active components) **222** fabricated in the bottom chip **220** are connected to microsystem devices **242** fabricated in a thin upper chip **240** by an interconnect structure **238** in a compliant interconnect layer **230**. *See* Application pages 9-10, and FIG. 3.

With regards to claims 3 and 6, Applicants teach that a thin interconnect layer (e.g., less than 50 microns) and a thin upper chip (e.g., less than 120 microns) are preferred to prevent thermal expansion mismatch between the stacked layers. *See* Application, page 9, lines 1-7, and page 10, lines 18-21.

Nowhere does *Okabe* teach or suggest a bottom chip, comprising one or more microsystem devices, and a thin upper chip, comprising one or more microsystem devices, connected to the bottom chip through an interconnect layer, as recited in Applicant's Claim 1. Accordingly, Applicants submit that this rejection is overcome and that Claim 1 is in condition for allowance. Furthermore, Applicant submits that Claims 3 to 7, 9, 11, and 12, that depend from and further define Claim 1, are likewise in condition for allowance. *See* MPEP 2143.03.

CONCLUSION

Applicant urges that the application is now in condition for allowance.

Respectfully submitted,

Kevin W. Bieg
Attorney for Applicant
Reg. No. 40,912
Ph: 505 284-4784
Sandia National Laboratories
P.O. Box 5800/MS 0161
Albuquerque, NM 87185-01

CERTIFICATION UNDER 37 CFR 1.8

I hereby certify that this correspondence and documents referred to herein were deposited with the United States Postal Service as first class mail addressed to: Commissioner for Patents, Alexandria, VA 22313-1450 on the date shown below.

Date: 7-18-06

By: Mary Loukota